


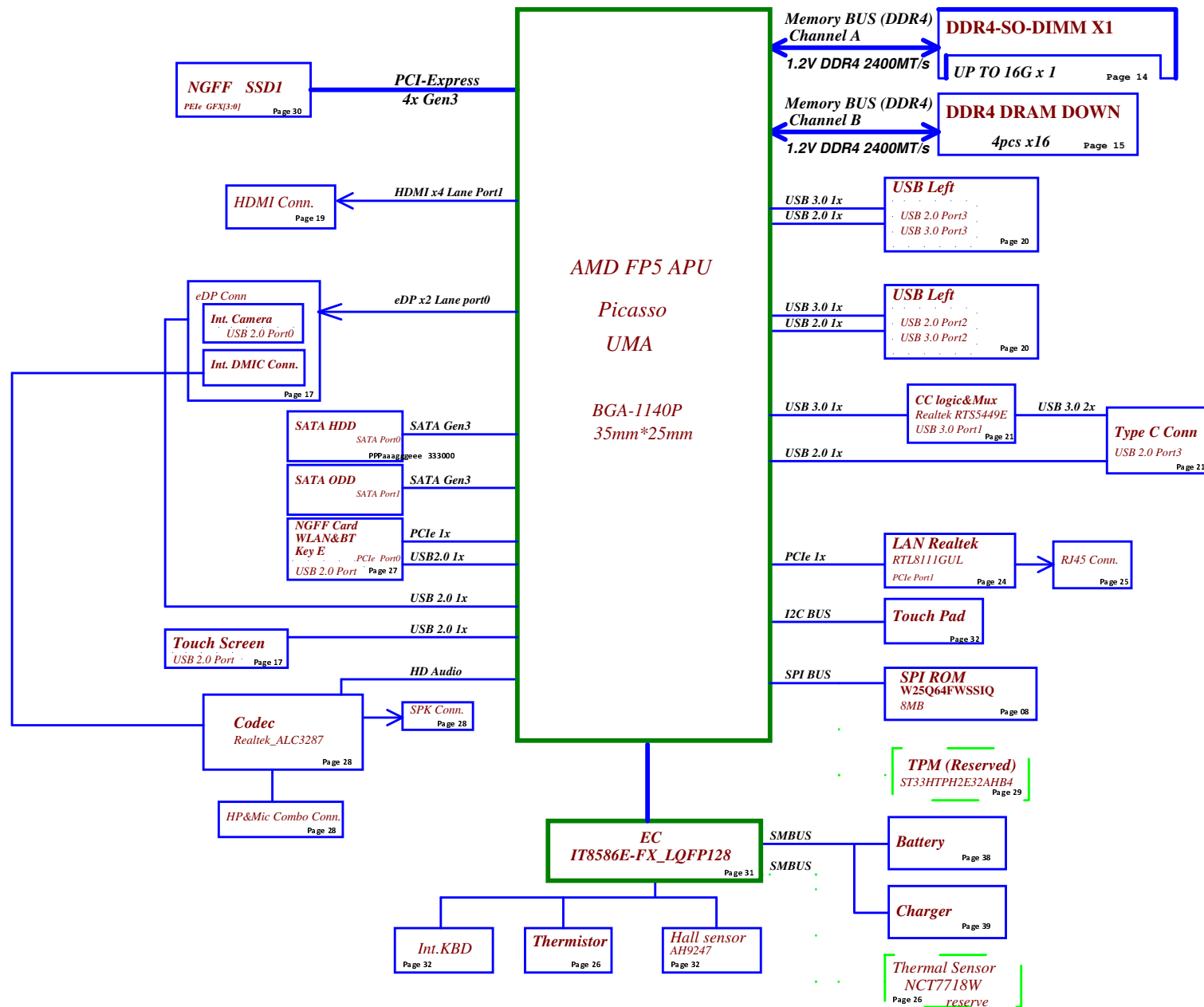
NM_C101 M/B Schematics Document

AMD FP5 PICASSO SOC with DDRIV

2018-12-29

REV:1.0

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			Document Number
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			0.3
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Voltage Rails (O --> Means ON , X --> Means OFF)

power plane	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_AFU) +1.8VALW +0.9VALW	+1.2V	+5VS +3VS +1.8VS +0.9VS +0.6VS +2.5VS +VDDC_VDD +VDDCR_SOC +VDDC +VDDCI +3VGS +1.8VGS +1.35VGS
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>S0 (Full ON)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S1 (Power On Suspend)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>LOW</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

I2C Control Table

	SOURCE	Device
TP_I2C0_SCL	APU	Touch Pad
TP_I2C0_SDA	+3VALW	+3VS

APU I2C address

Device	Address
Elan: SA469D-22HA 69x104x1.0	?
Synaptics: TM-P3255-008 69x104x1.0	?

SMBUS Control Table

	SOURCE	GPU	BATT	IT8586	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC
EC_SMB_CK1 EC_SMB_DA1	IT8586 +3VL	X	V		X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8586 +3VL	X	X		X	X	V +3VS	X	X	V
EC_SMB_CK3 EC_SMB_DA3	IT8586 +3VS	V +3VS_VGA	X		X	X	X	V	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X		X	X

EC SM Bus1 address

Device	Address
Battery	?
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
PMIC	0X34
Thermal Sensor	1001_100xb(reserv

EC SM Bus3 address

Device	Address
GPU	0x41(default)
APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting

APU SM Bus address


Device	Address
DDR4 SO-DIMM	?
WLAN	RSVD

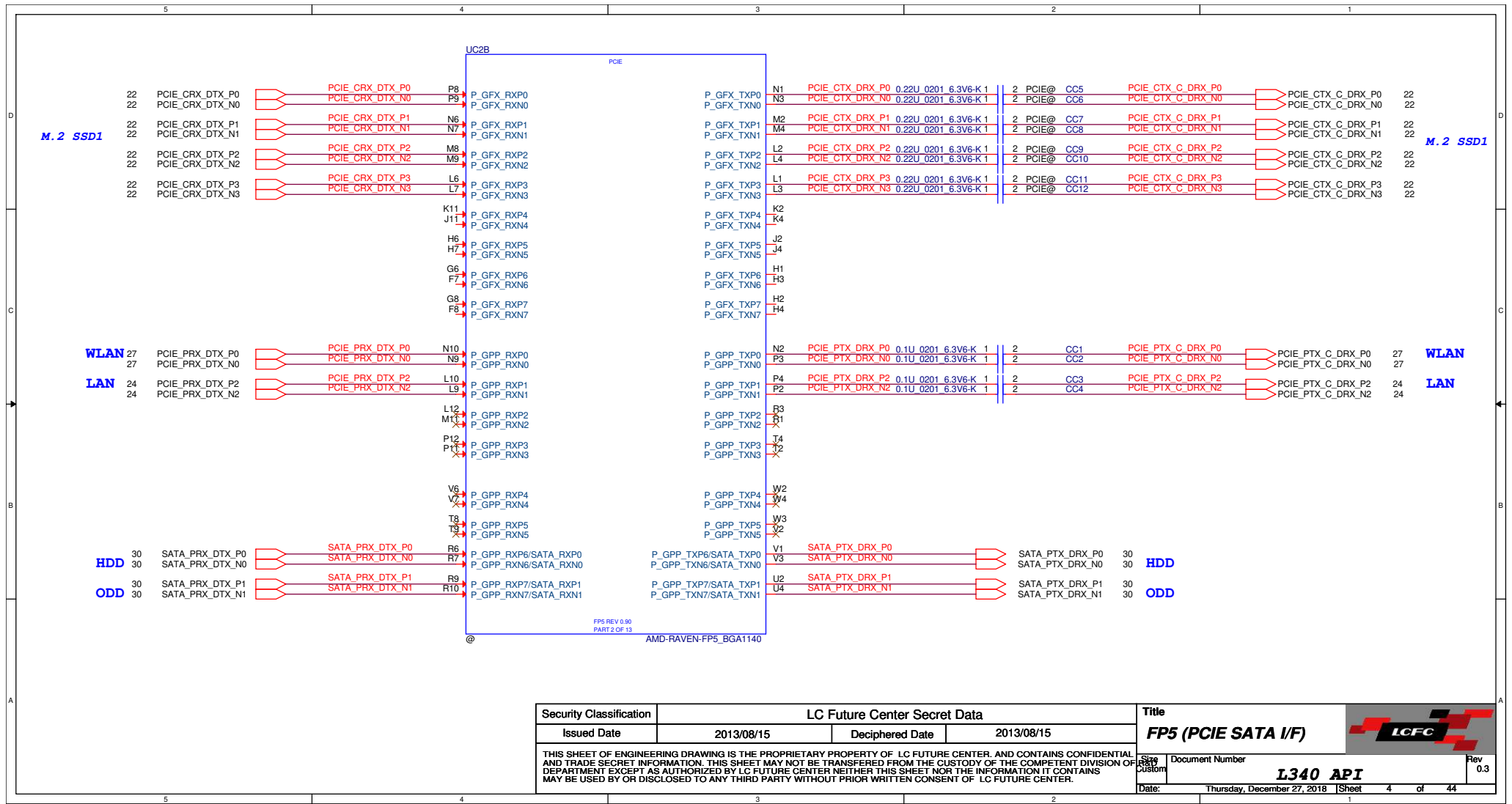
Port List


HSIO Port		Device
GPP	0	WLAN
	1	LAN
	2	N/A
	3	N/A
	4	N/A
	5	N/A
	6	HDD
	7	ODD
GFX	0	SSD
	1	
	2	
	3	
	4	
	5	
	6	
	7	
USB3.0	0	N/A
	1	Type C
	2	LEFT USB (3.0) lower
	3	LEFT USB (3.0) upper
	4	N/A
USB2.0	0	Camera
	1	Type C
	2	LEFT USB (3.0) lower
	3	LEFT USB (3.0) upper
	4	Touch
	5	BT

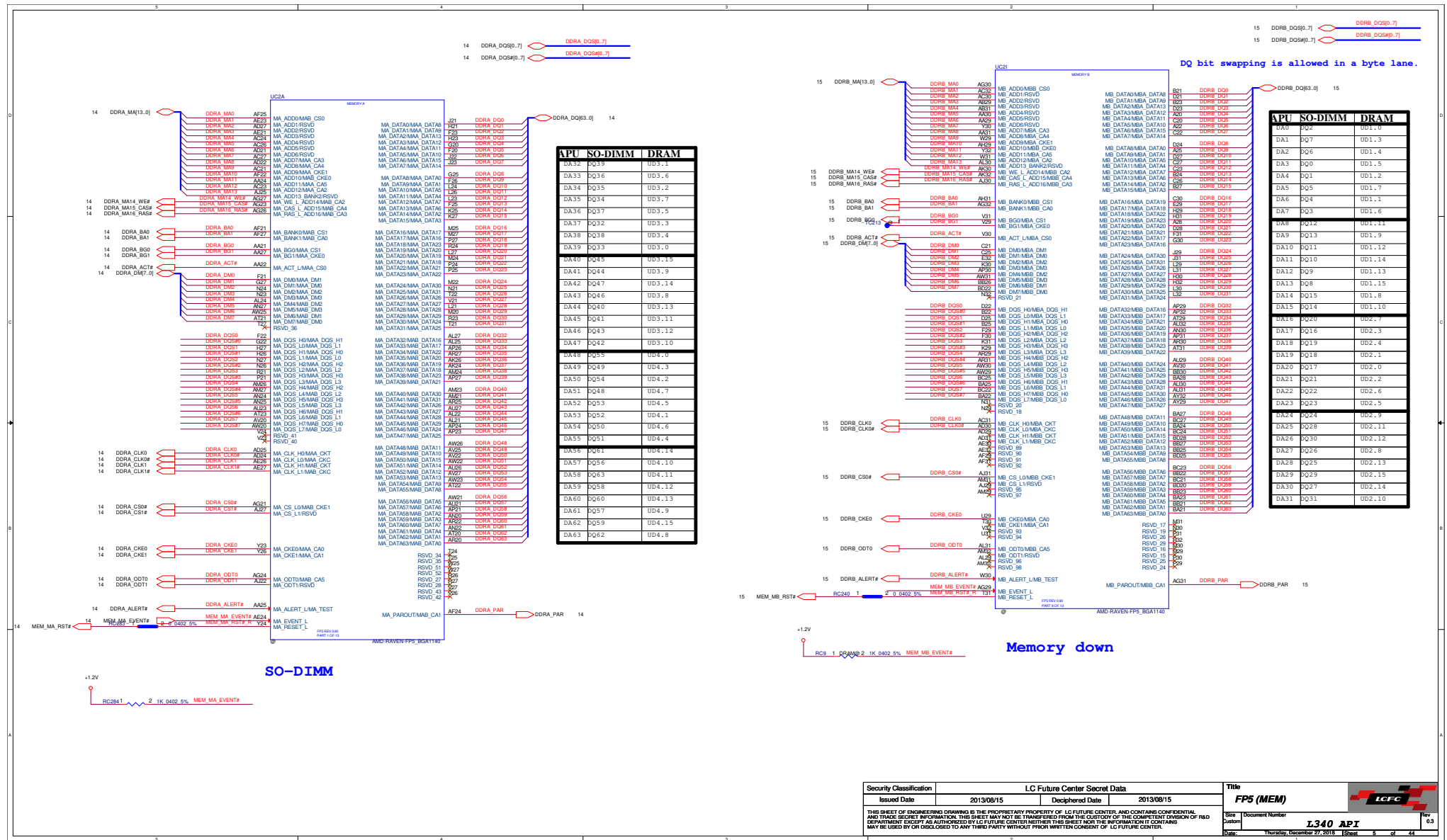
BOM Structure Table


[illegible]

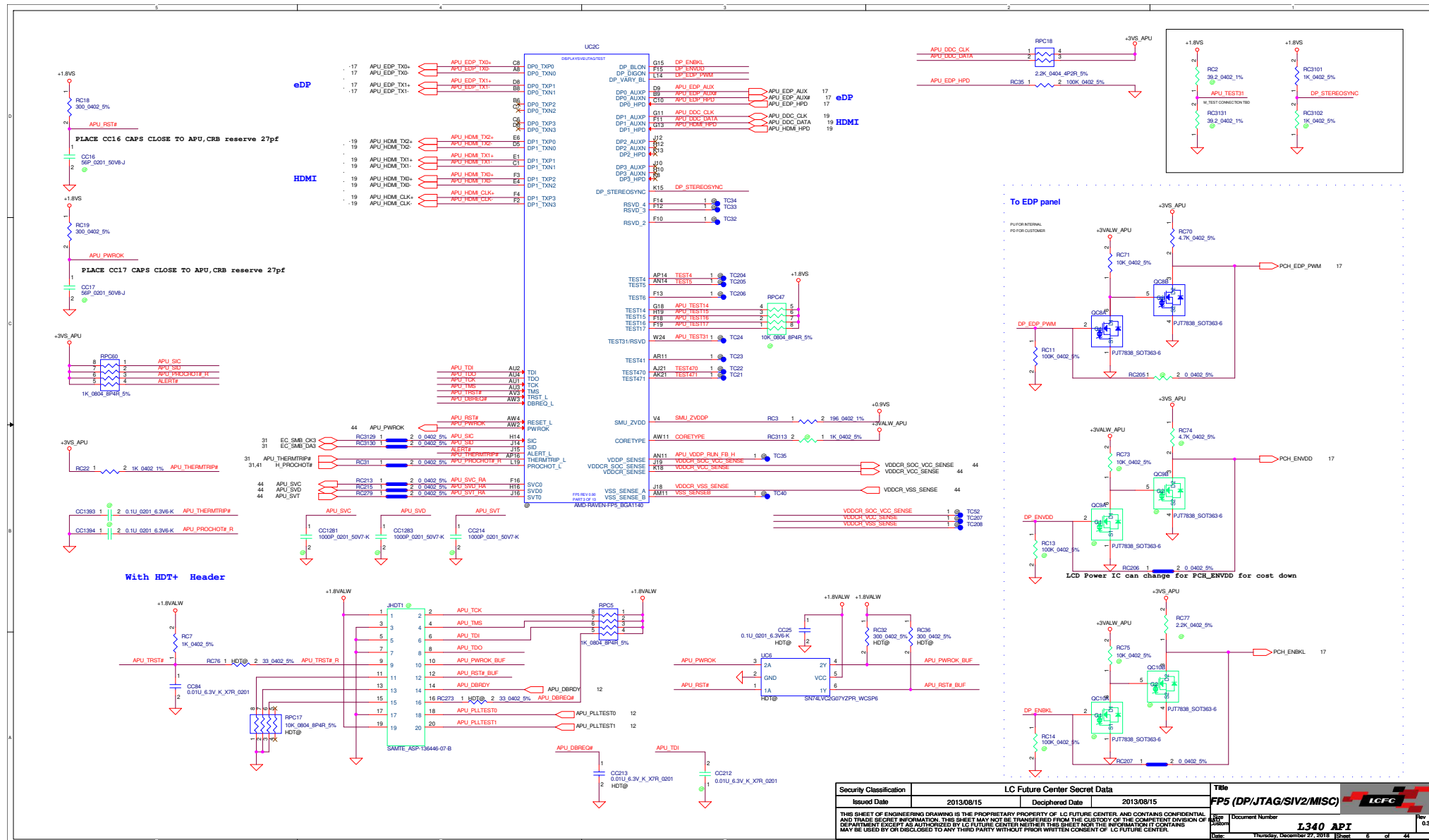
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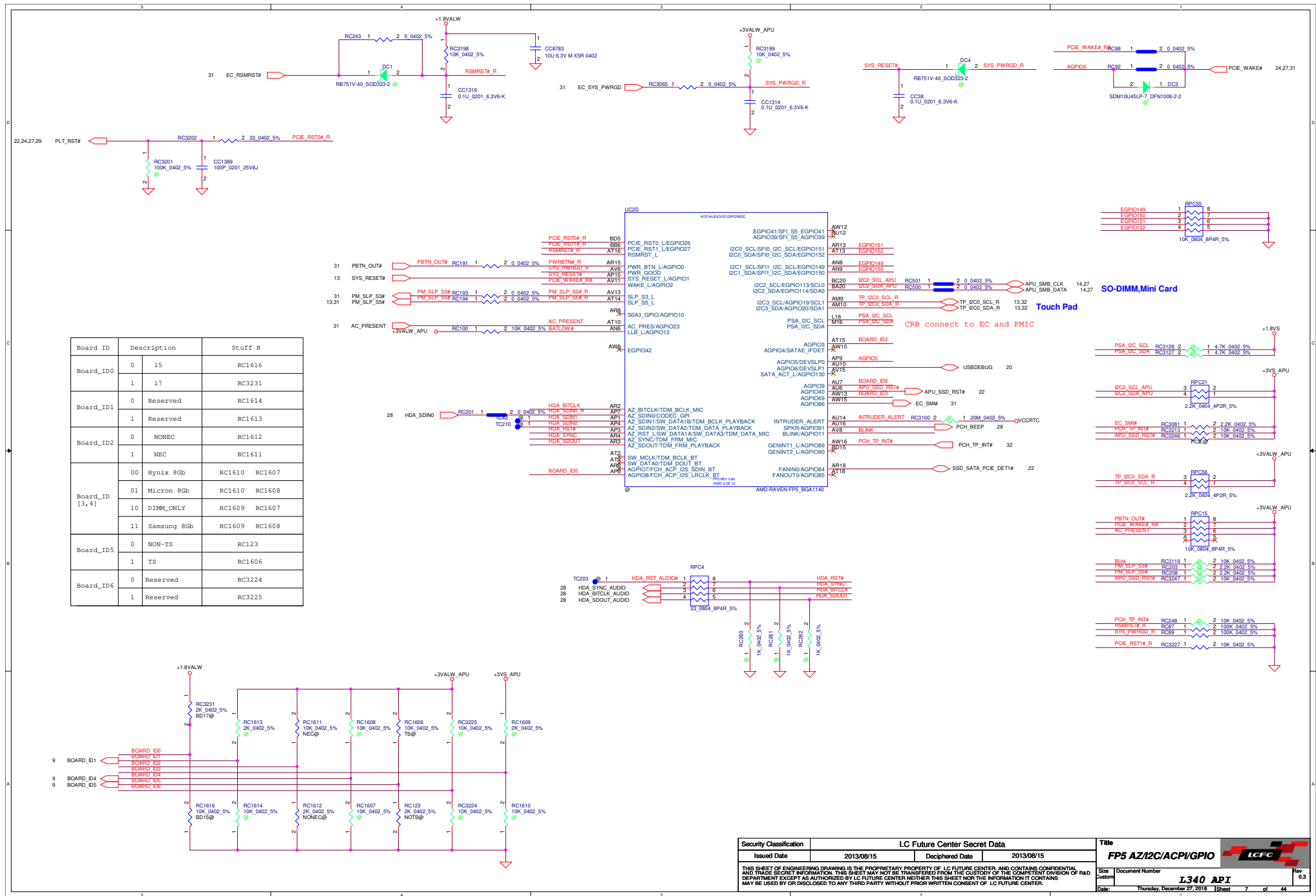
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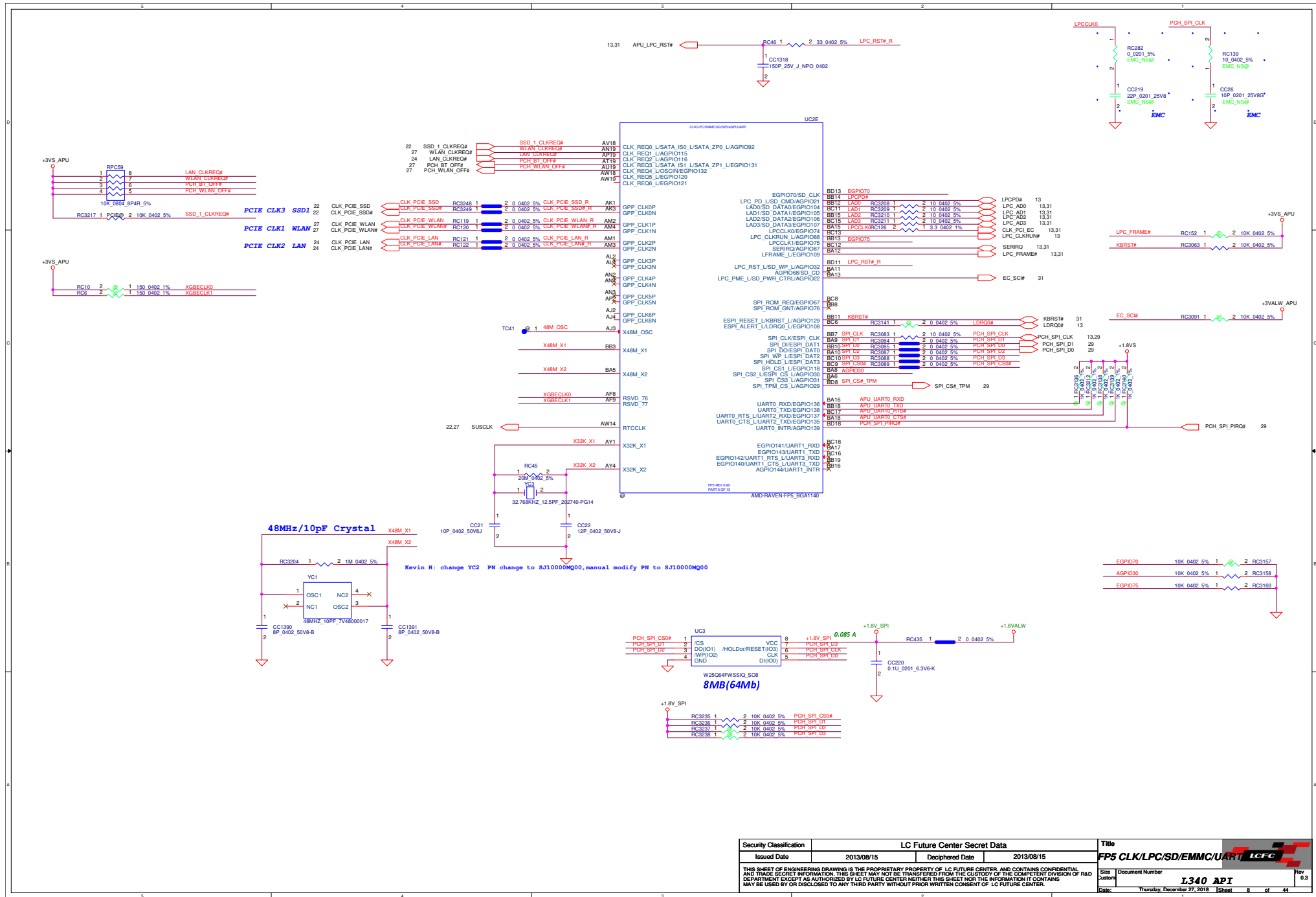


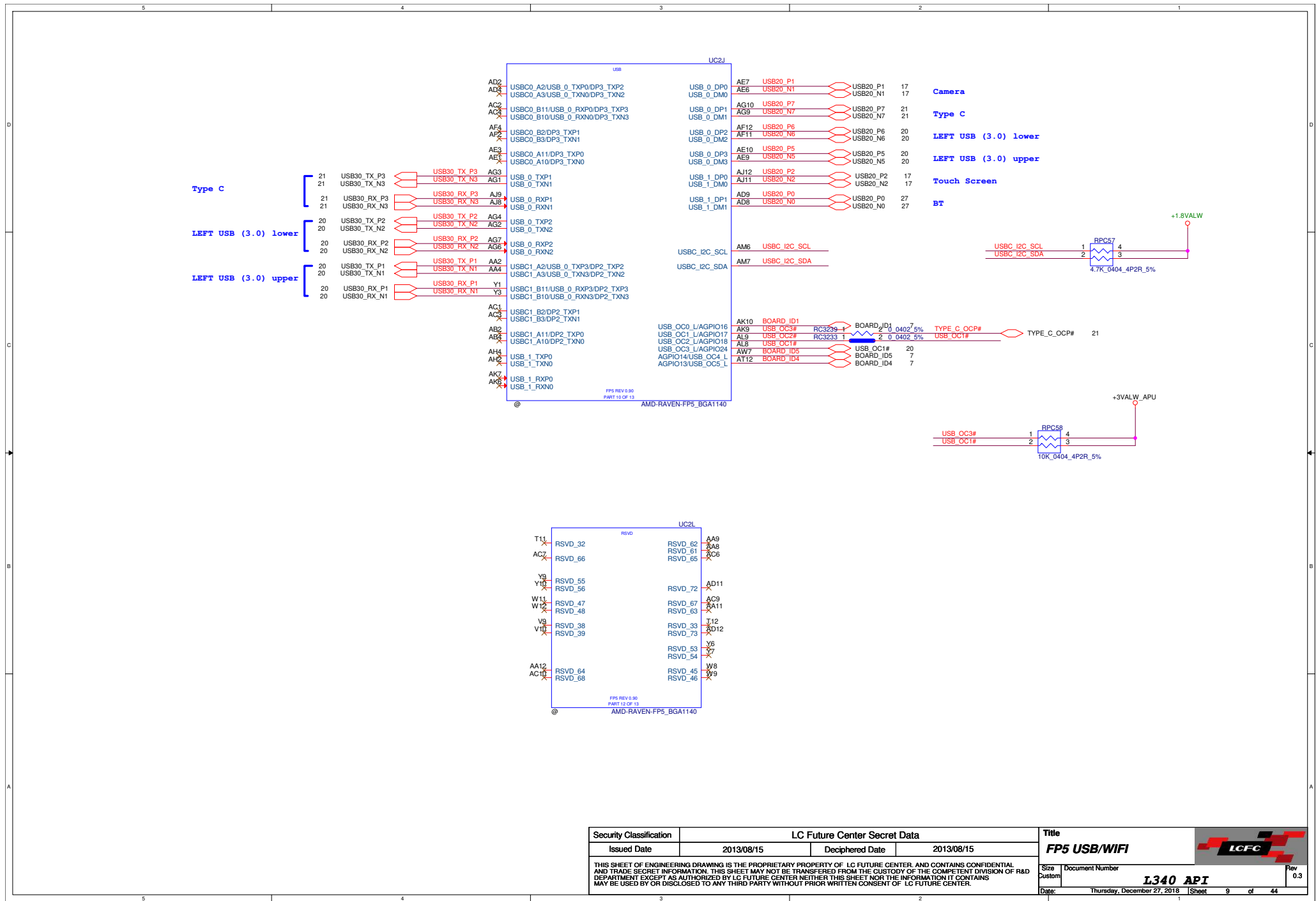
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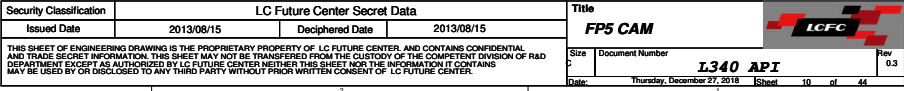


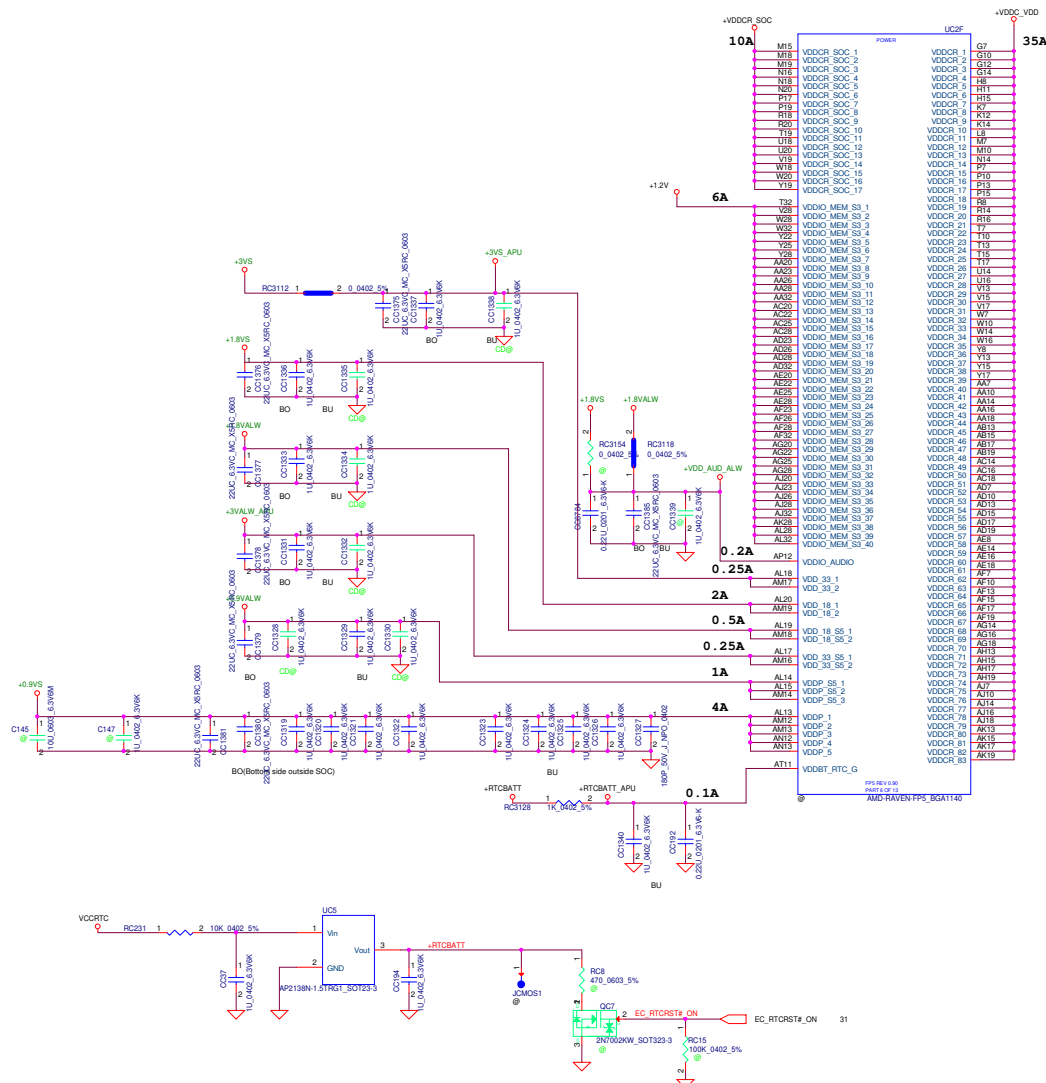
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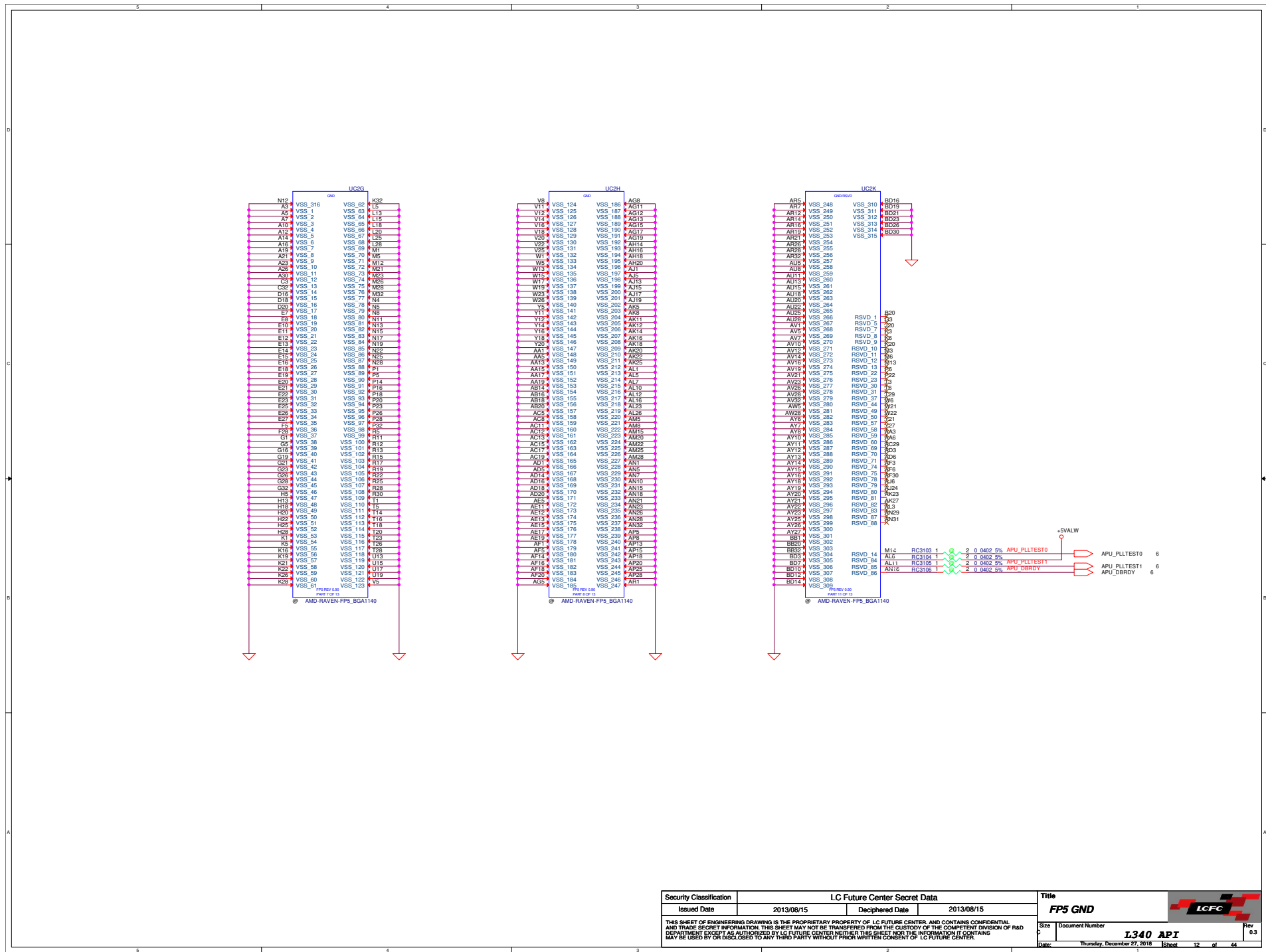


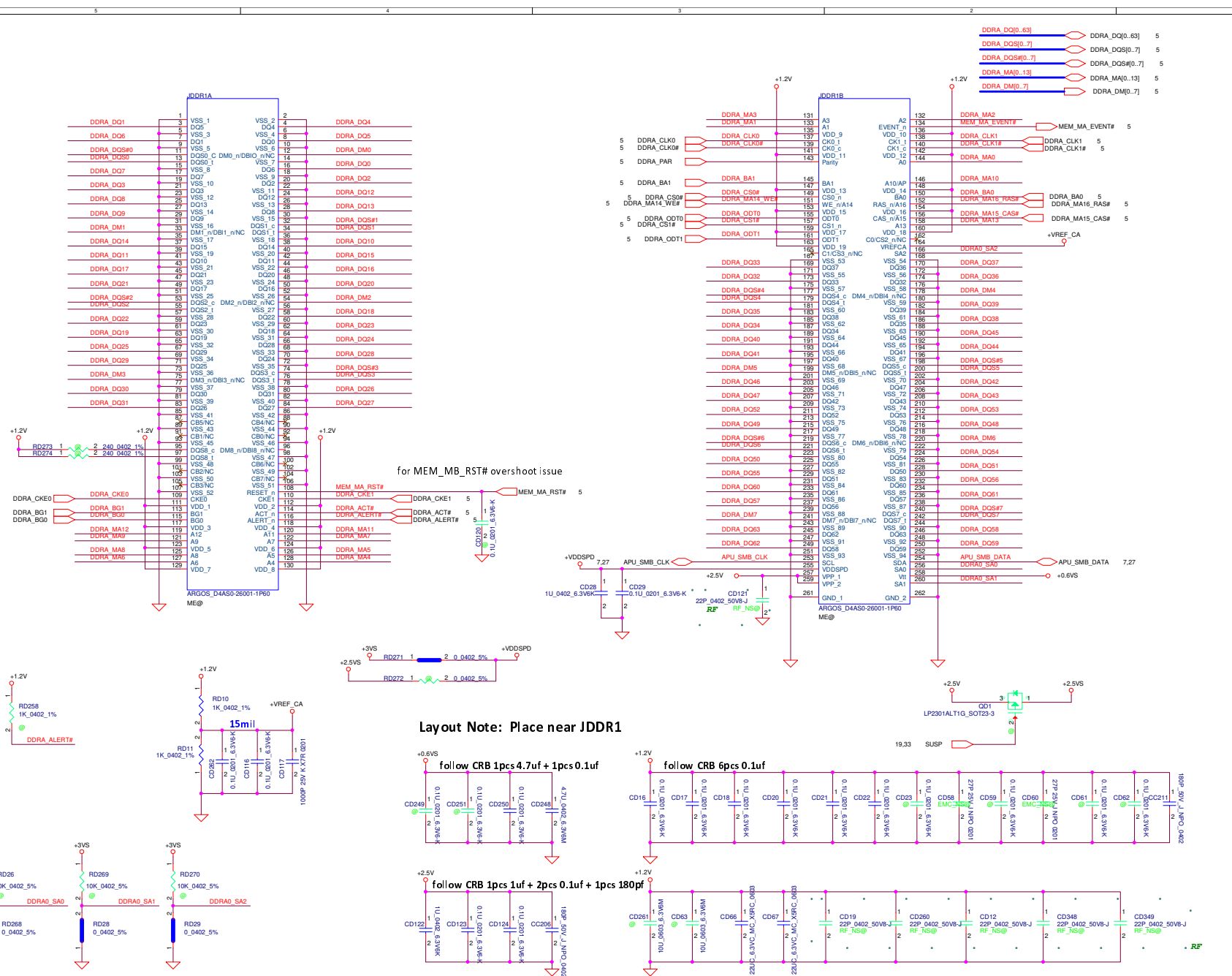




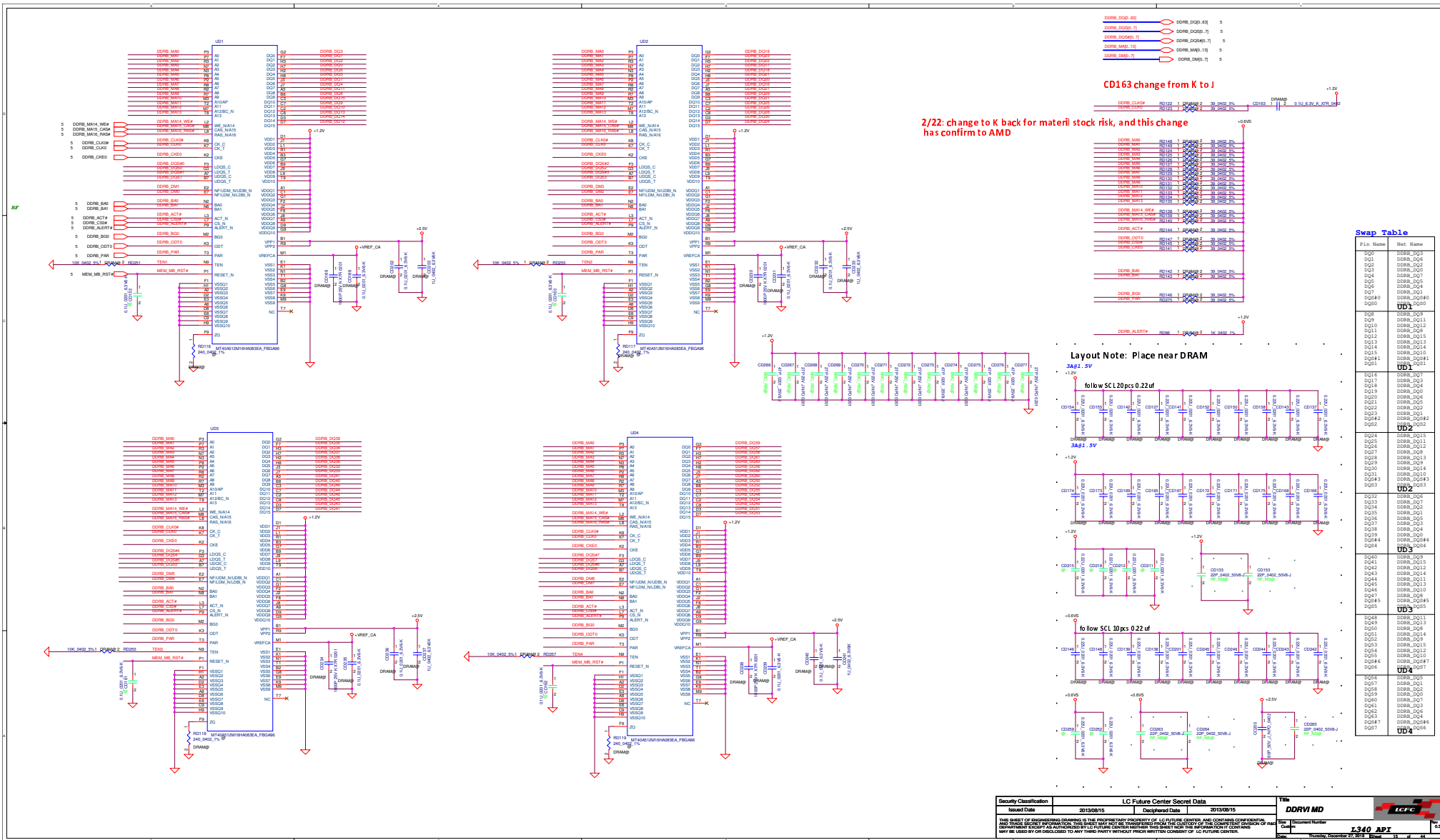




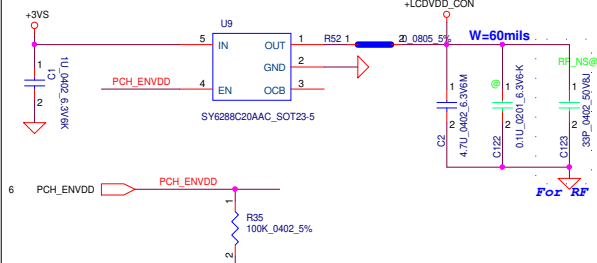




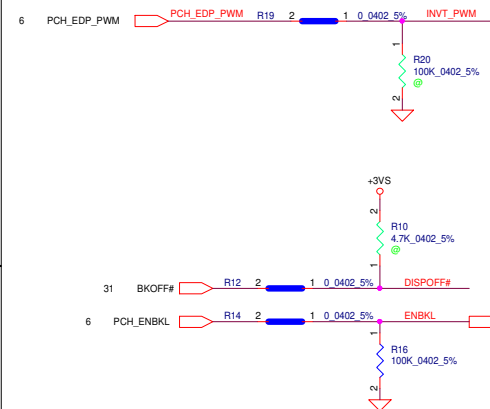
SPD Address = A2H



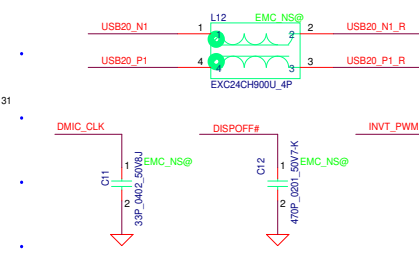
LCD POWER CIRCUIT



APU output enable Voh min is 1.8V-0.45V=1.35V

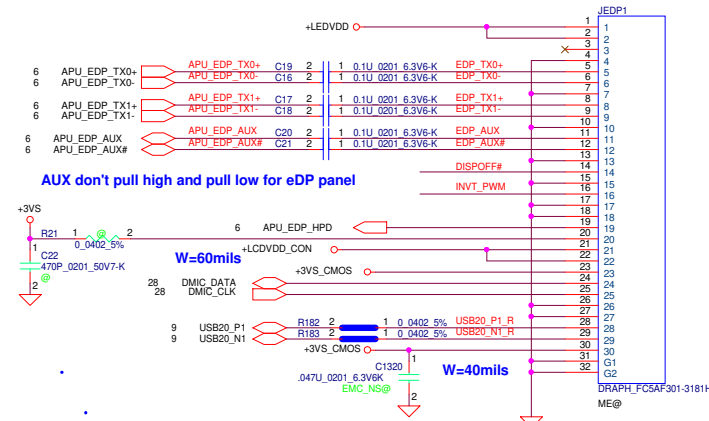
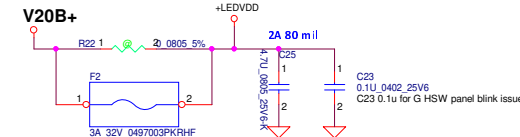


CMOS Camera

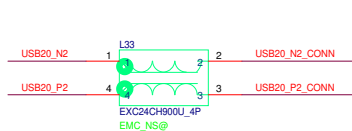


Touch Screen

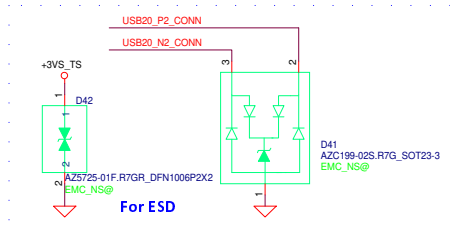
B+ to +LEDVDD POWER



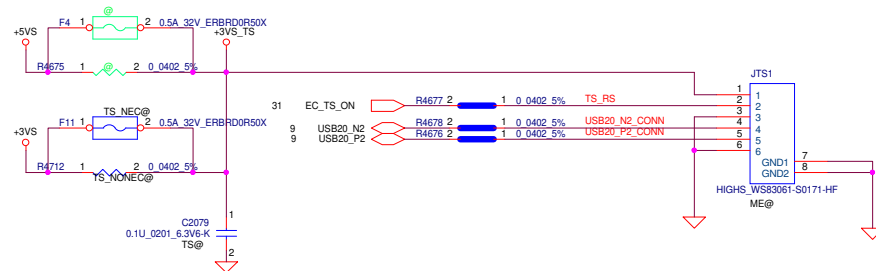
Touch Screen



For EMI

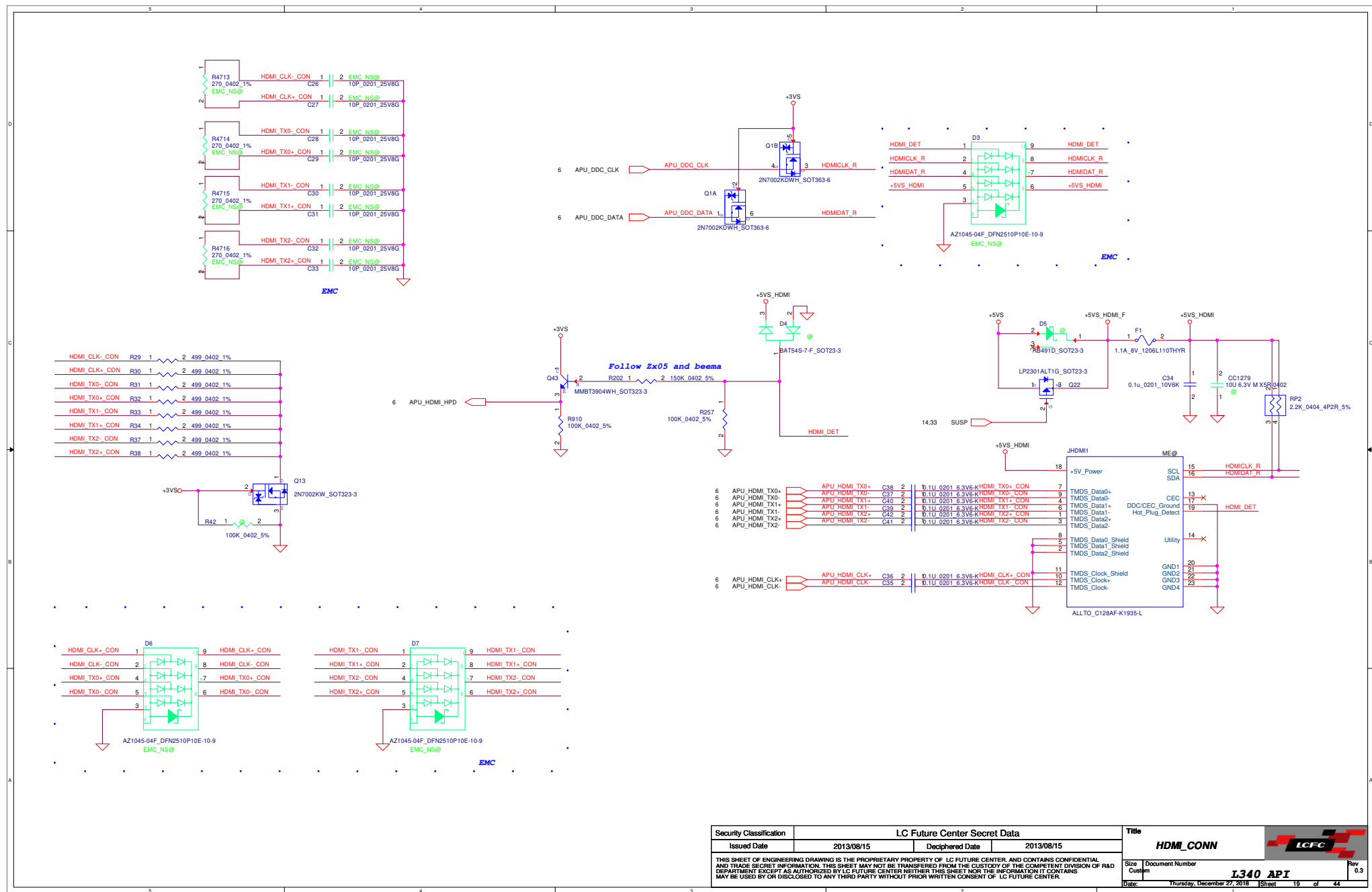


For ESD

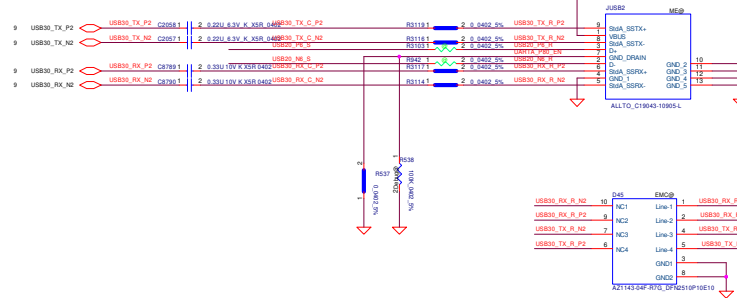
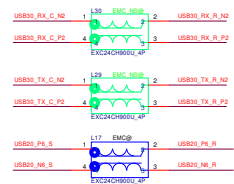
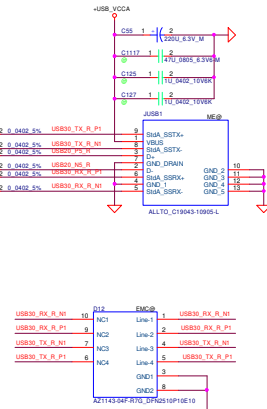
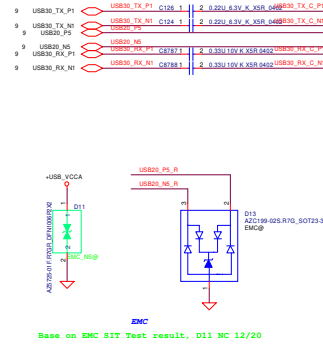
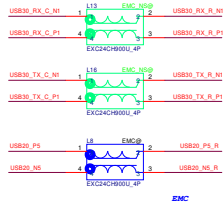
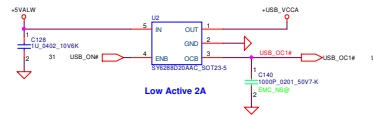


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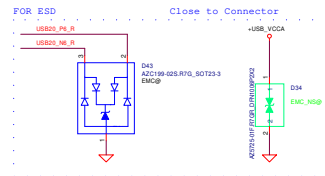
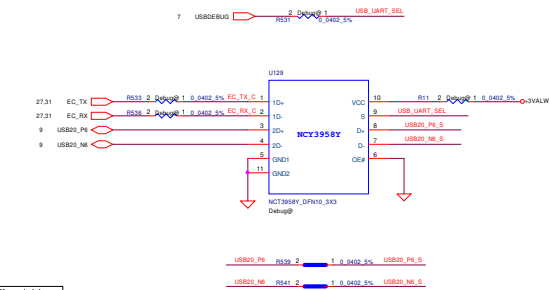
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LEFT SIDE USB3.0 PORT x2



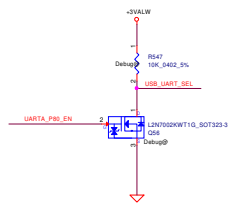
For USB Debug Function



USBDEBUG	Kernel debug
USBDEBUG	Kernel debug
USBDEBUG	Kernel debug

JTAG_P80_EN	POST 80
JTAG_P80_EN	POST 80
JTAG_P80_EN	POST 80


SOFT FUNCTION	SOFT FUNCTION
SOFT FUNCTION	SOFT FUNCTION
SOFT FUNCTION	SOFT FUNCTION



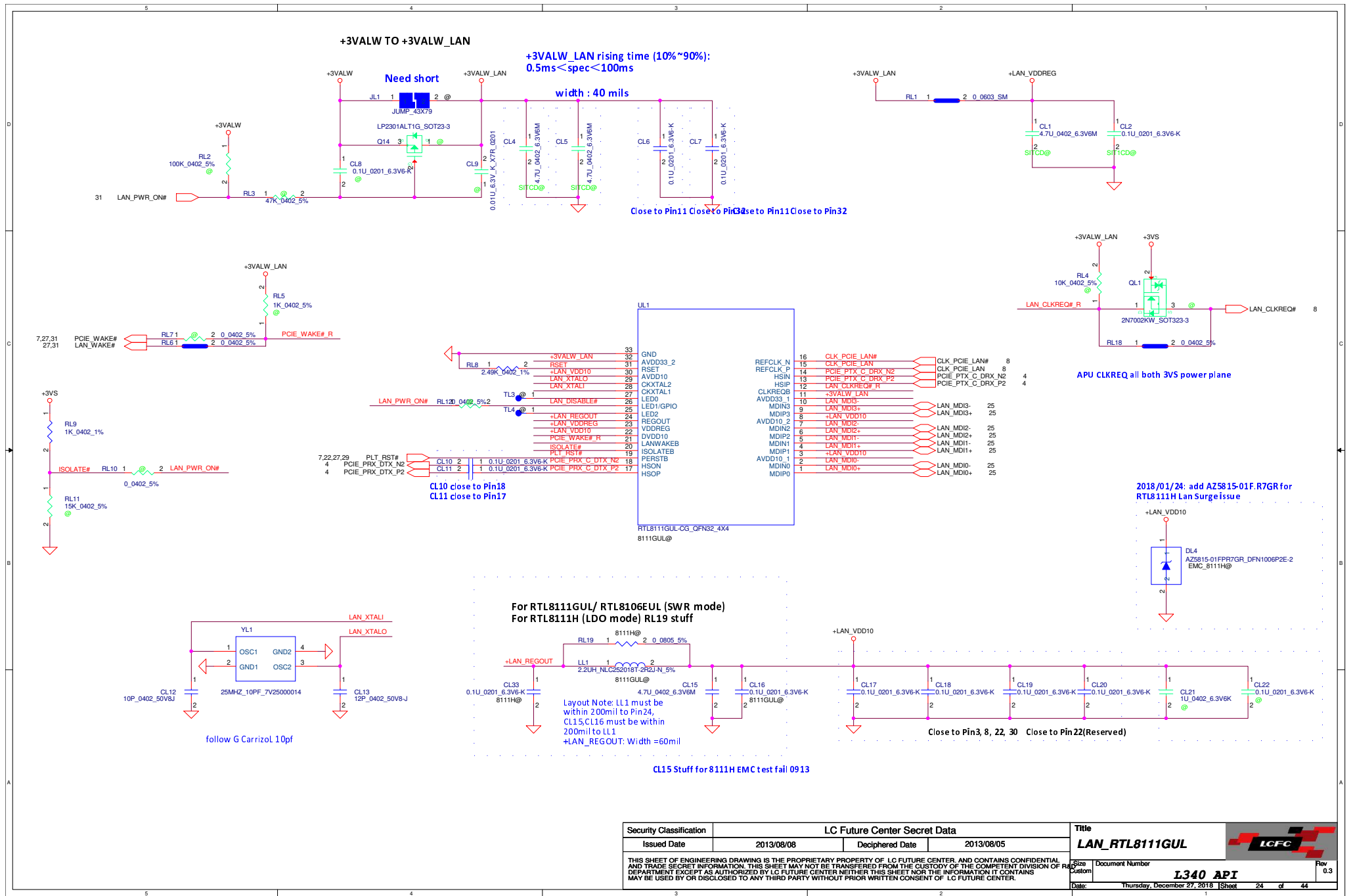
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Deciphered Date	2017/08/16

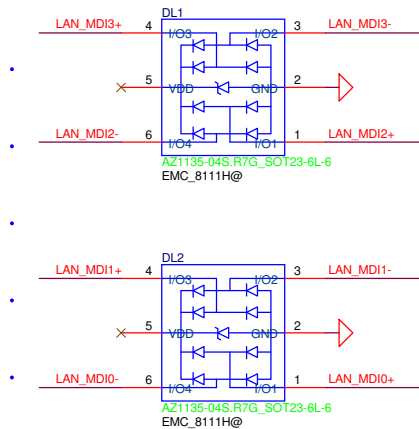
Title	USB3.0 PORT (LEFT)
Document Number	1.340 APT
Version	1.0



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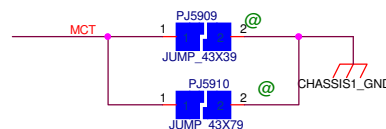
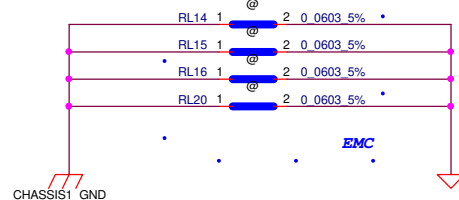
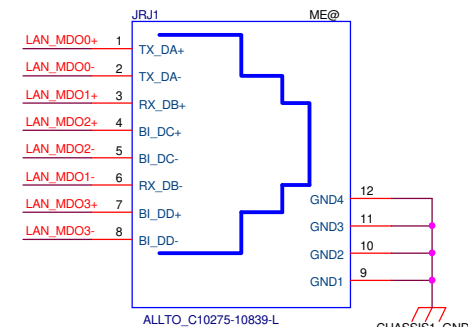
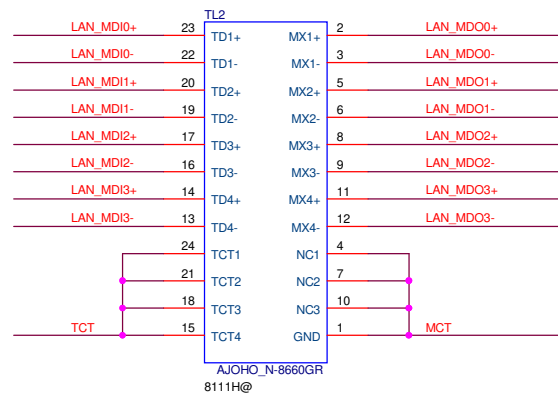
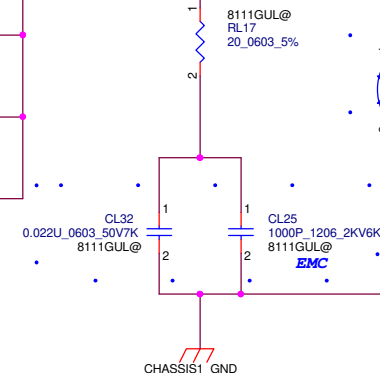
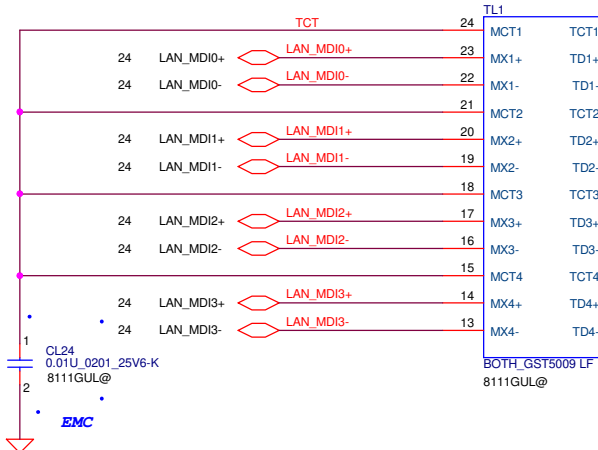
5					4					3					2					1				
D																								
C																								
B																								
A																								





Place Close to TL1
Change part number

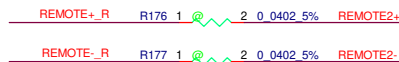
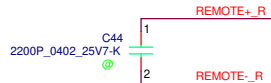
EMC



add PJ5910 for 8111H EMC test fail 0913

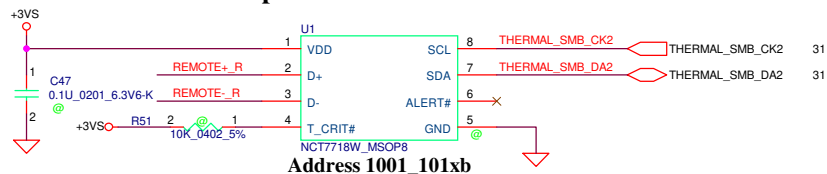
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Close to U1

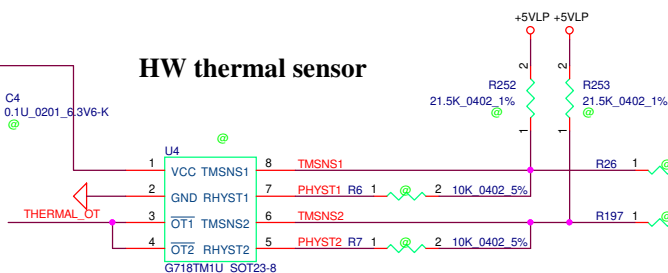


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM

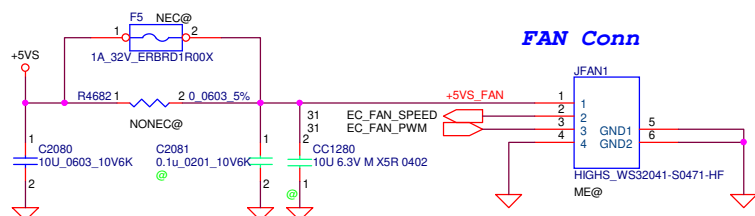


HW thermal sensor

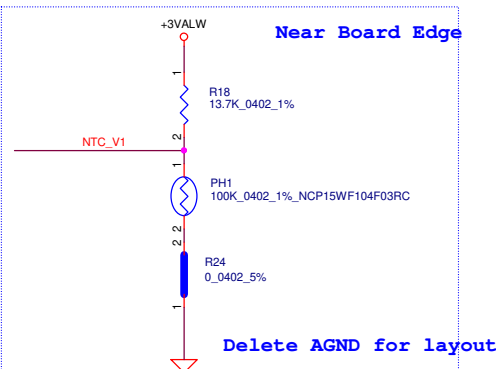


over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML) / (3*RTML-RSET)
56+/-30C

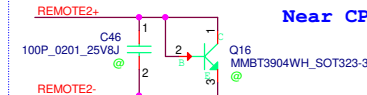
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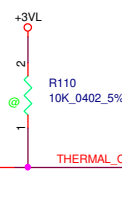
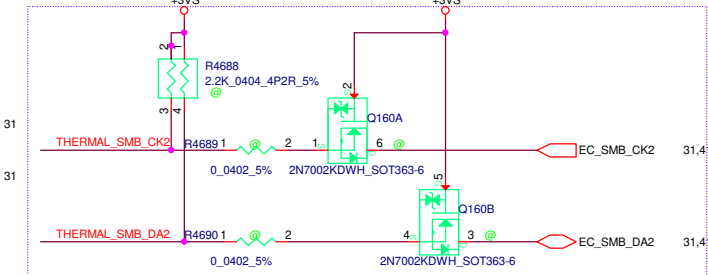
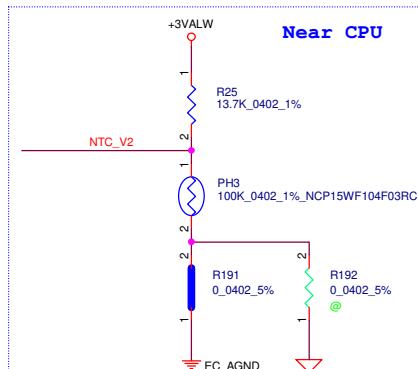
Near Board Edge



Near CPU core

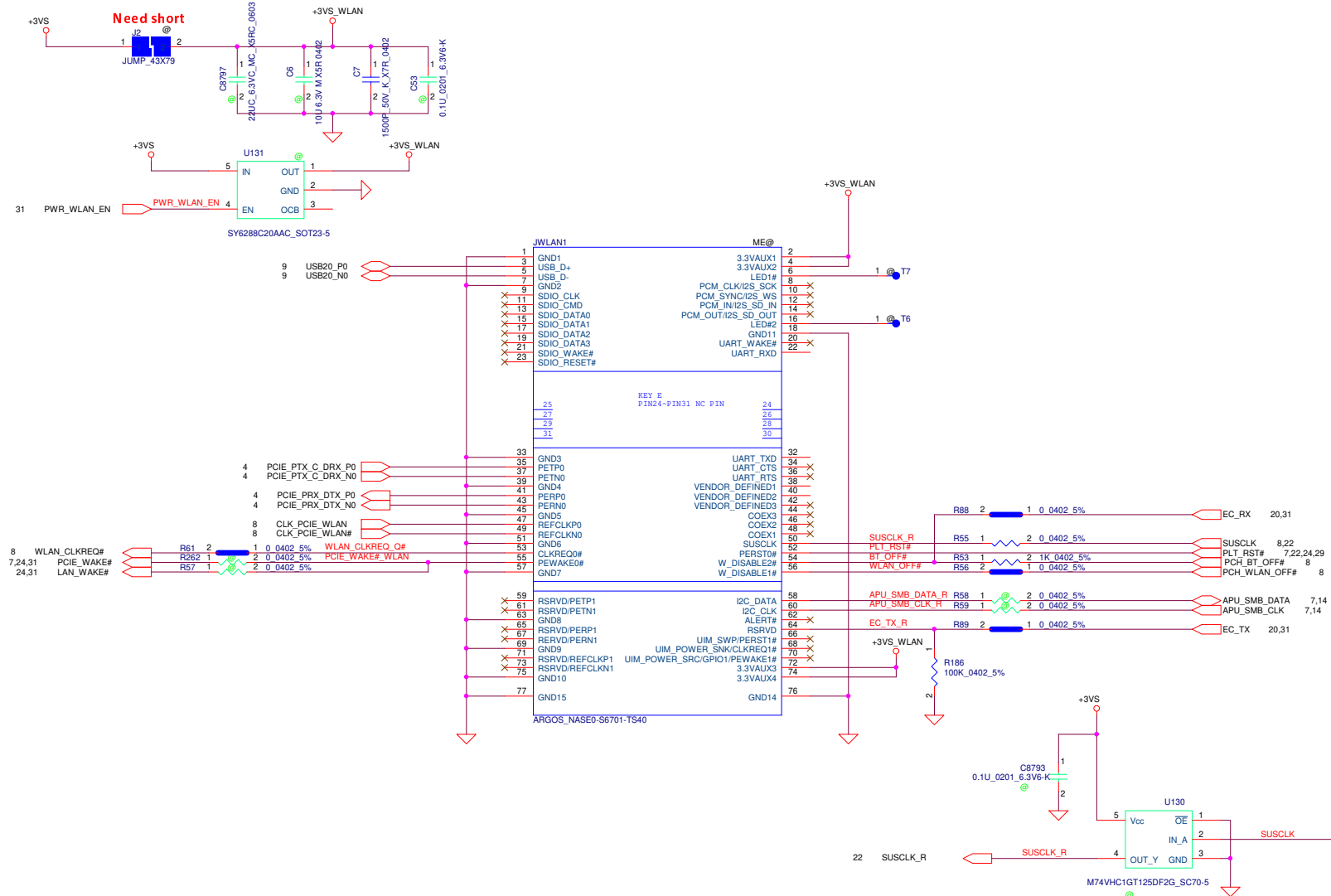


Near CPU

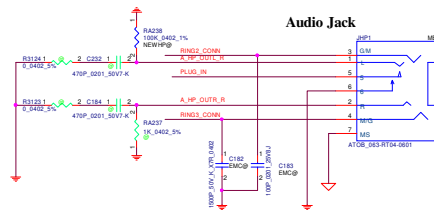


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Mini-Express Card(WLAN/WiMAX)

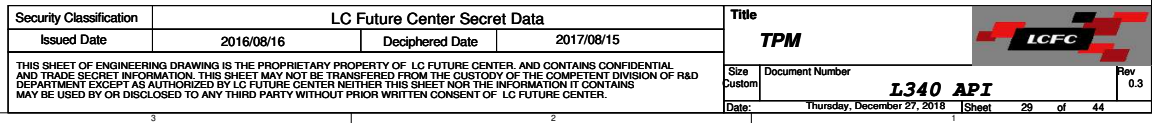


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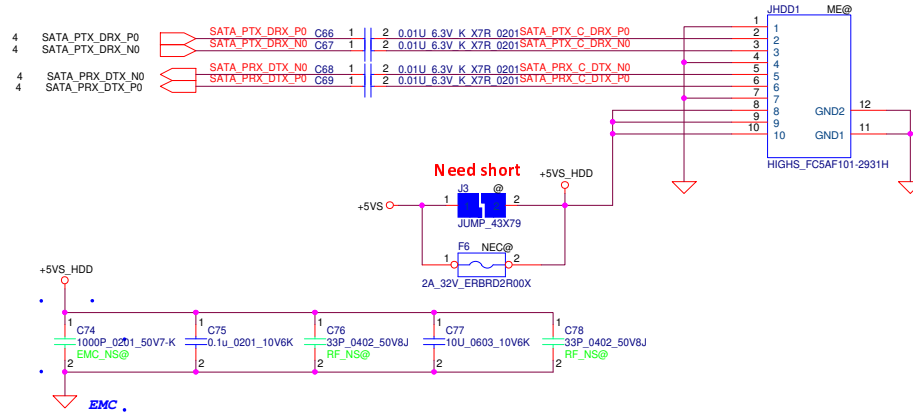


```
Verb table configures as 1 JD
mode with internal 47k pull
high to save external ROM.
new Audio Jack: Verb table configures as 2 JD
mode
Follow realtek suggest, change CA205 to 0.22u
```

Reserve for L34 0API SPKR EMC noise 0912



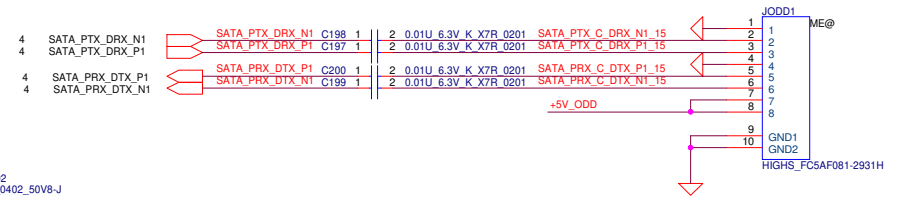
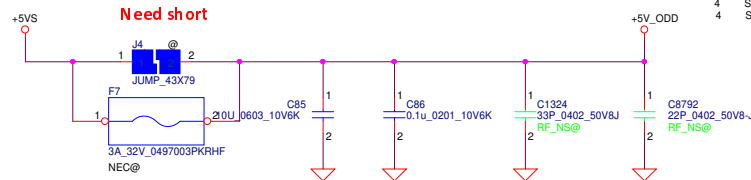
SATA HDD Conn.



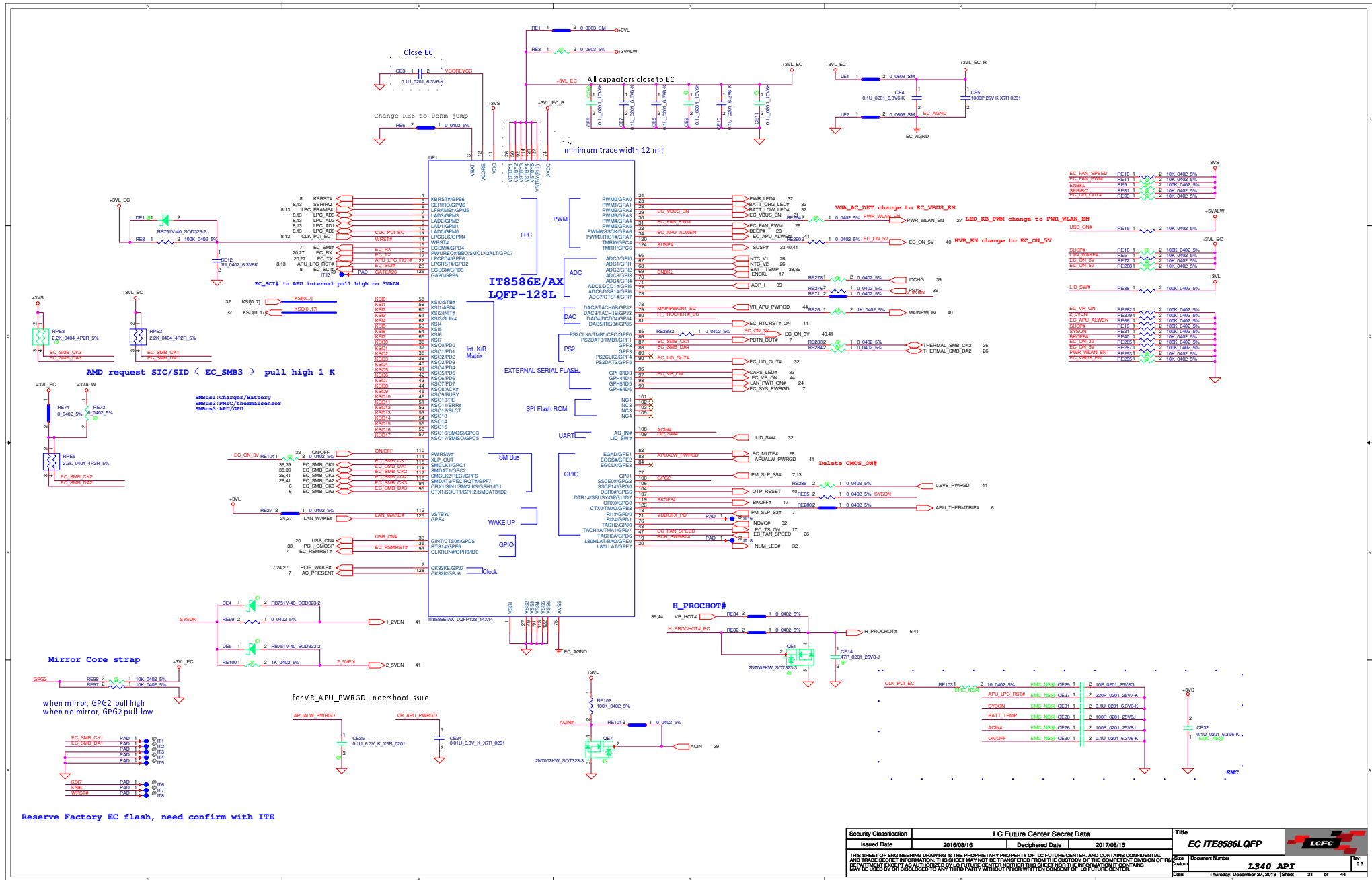
FOR 15"
SATA ODD FFC Conn

SATA 15 ODD P/N pin assign is different from G SKL

+5VS to +5V_ODD



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[illegible]

The schematic diagram illustrates the internal components of the NOVO BTM module. It features a 5W2 vacuum tube (6-pin package) and a 625A diode (4-pin package). The 5W2 tube is connected to a 100K resistor and a 100V source. The output of the tube is connected to the diode, which is also connected to a 100K resistor and a 100V source. The output of the diode is labeled NOVO BTM.

[illegible]

The schematic diagram illustrates the power supply configuration for the 6 SA 32V_EBR0R050X. It features three parallel power rails: PWR_LEDA, CAPS_LEDA, and PWR_LEDB. Each rail is connected to a 200,0402-1% resistor (R274, R275, R276) and a 200,0402-5% resistor (R277, R278, R279). The PWR_LEDA rail is connected to a 200,0402-1% resistor (R274) and a 200,0402-5% resistor (R277). The CAPS_LEDA rail is connected to a 200,0402-1% resistor (R275) and a 200,0402-5% resistor (R278). The PWR_LEDB rail is connected to a 200,0402-1% resistor (R276) and a 200,0402-5% resistor (R279). The diagram also shows the connection of the power supply to the 6 SA 32V_EBR0R050X component.


[illegible]

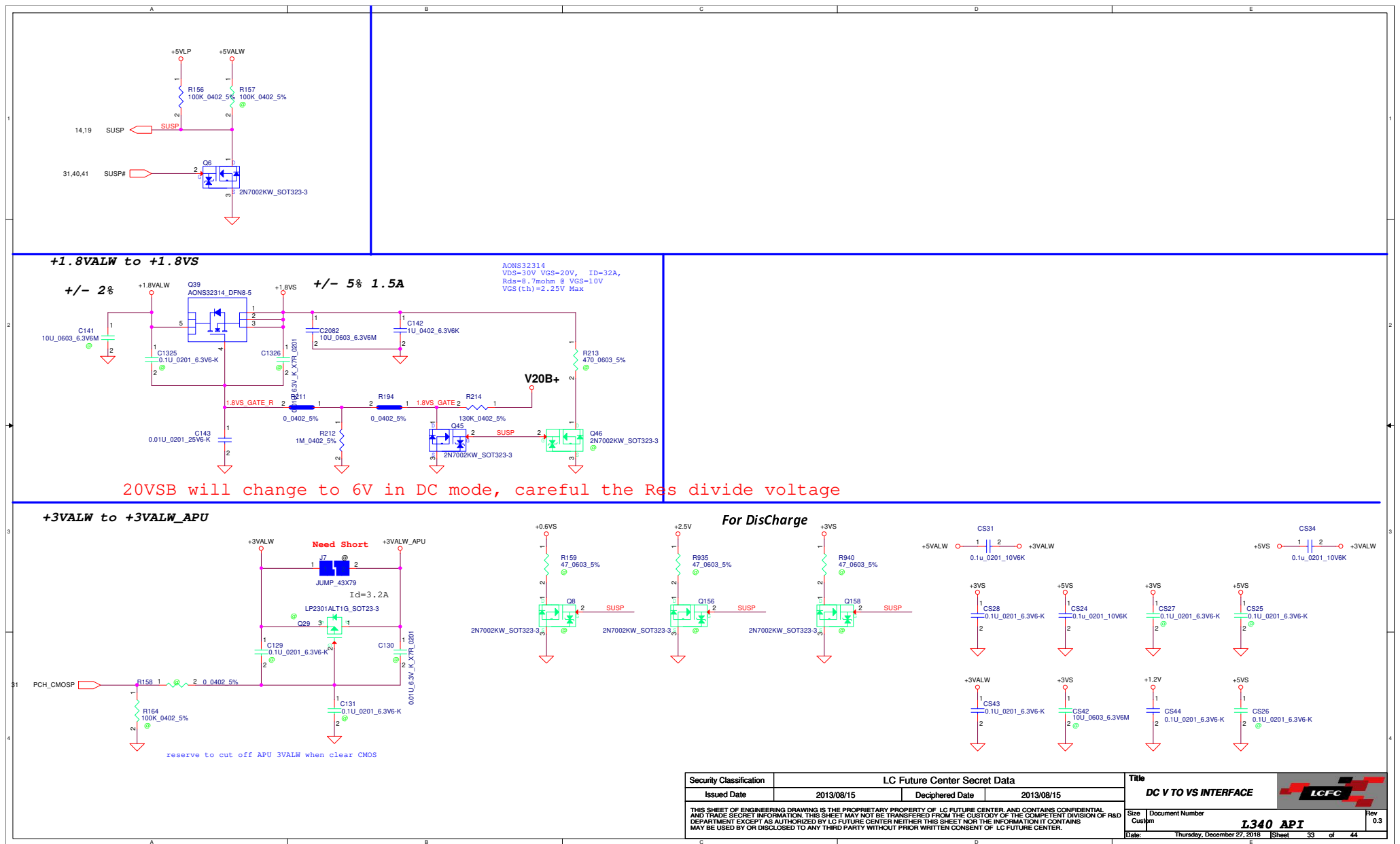
TP/B Connector

TP1_MEQ

TP1_MEQ

TP1_MEQ

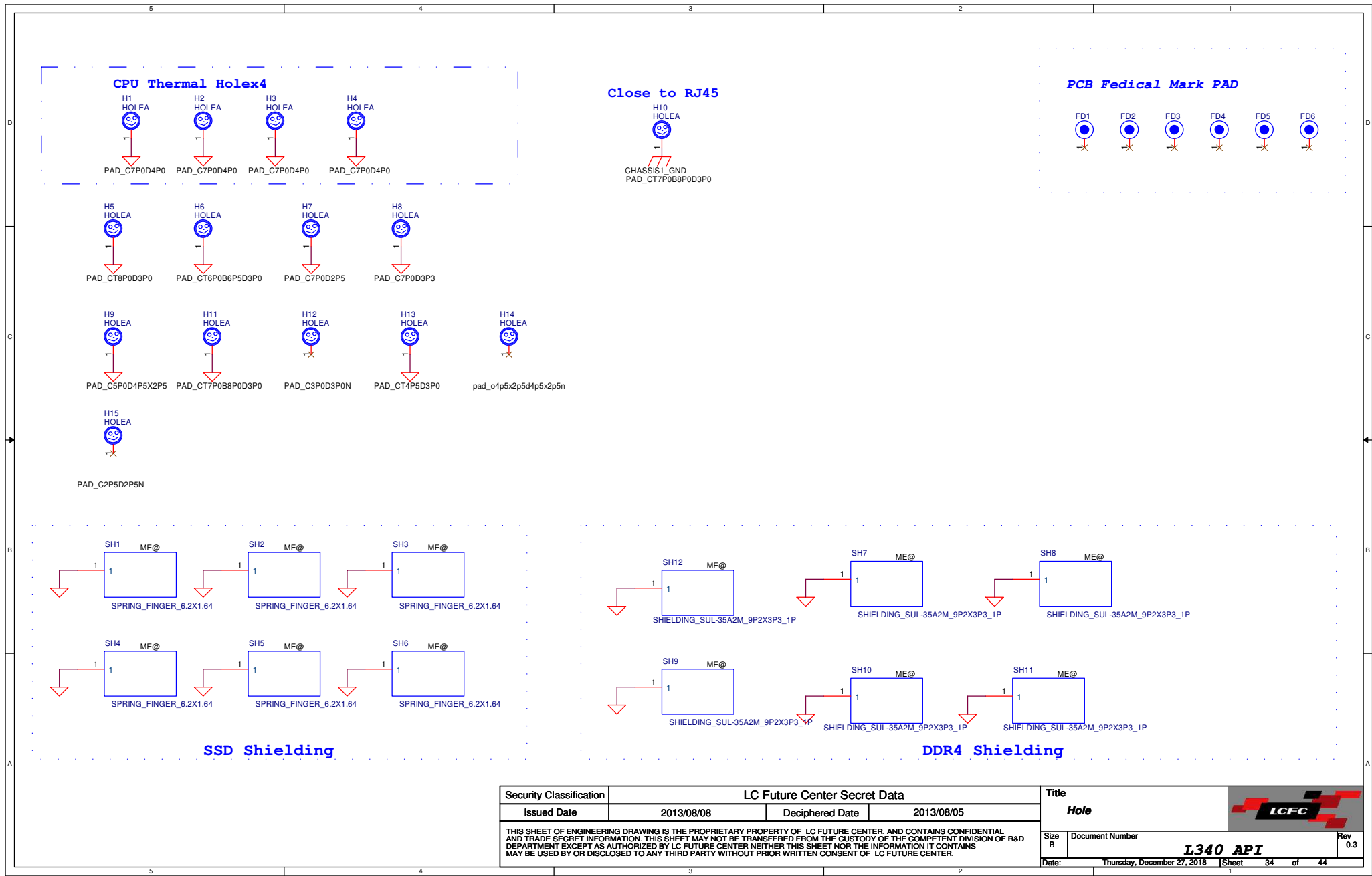
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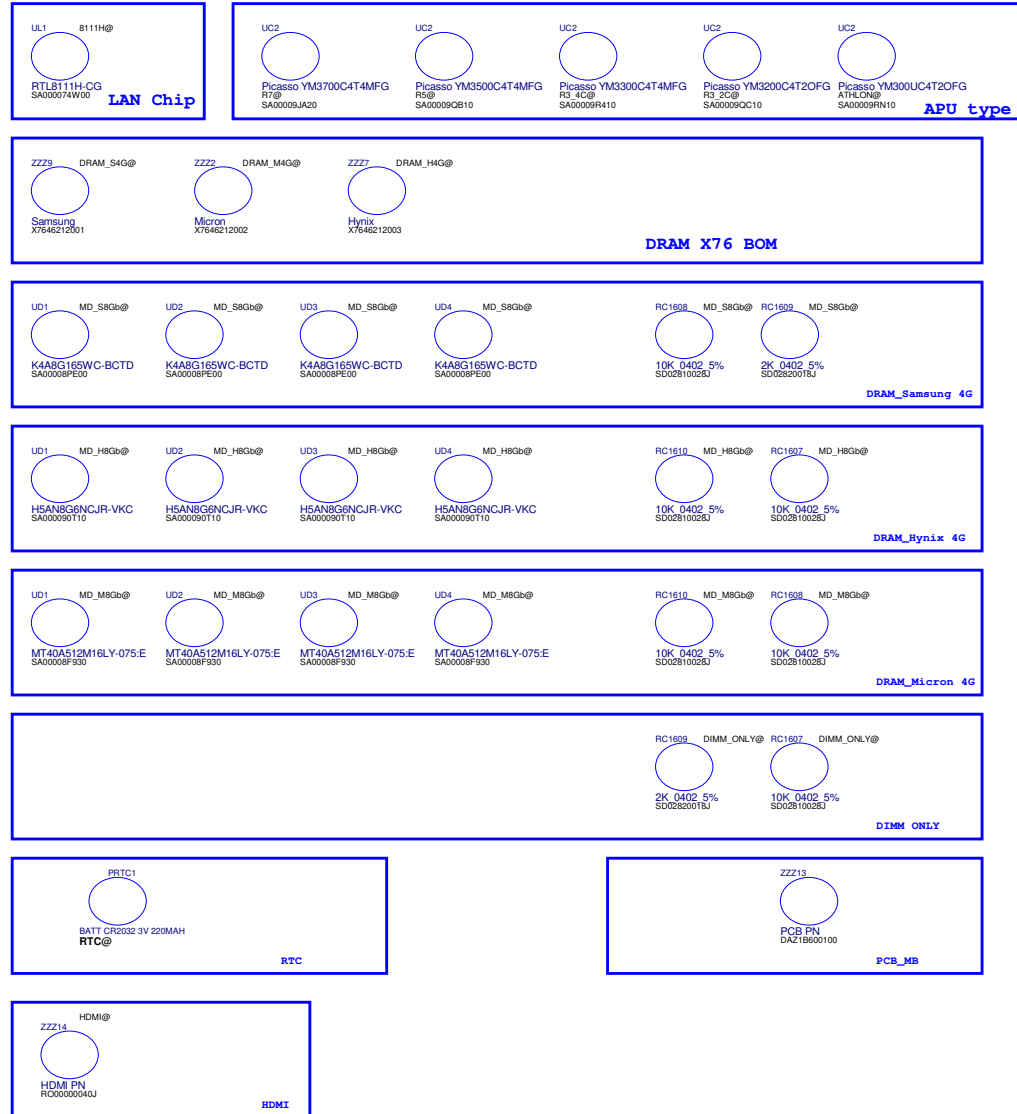


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				Sheet	33 of 44



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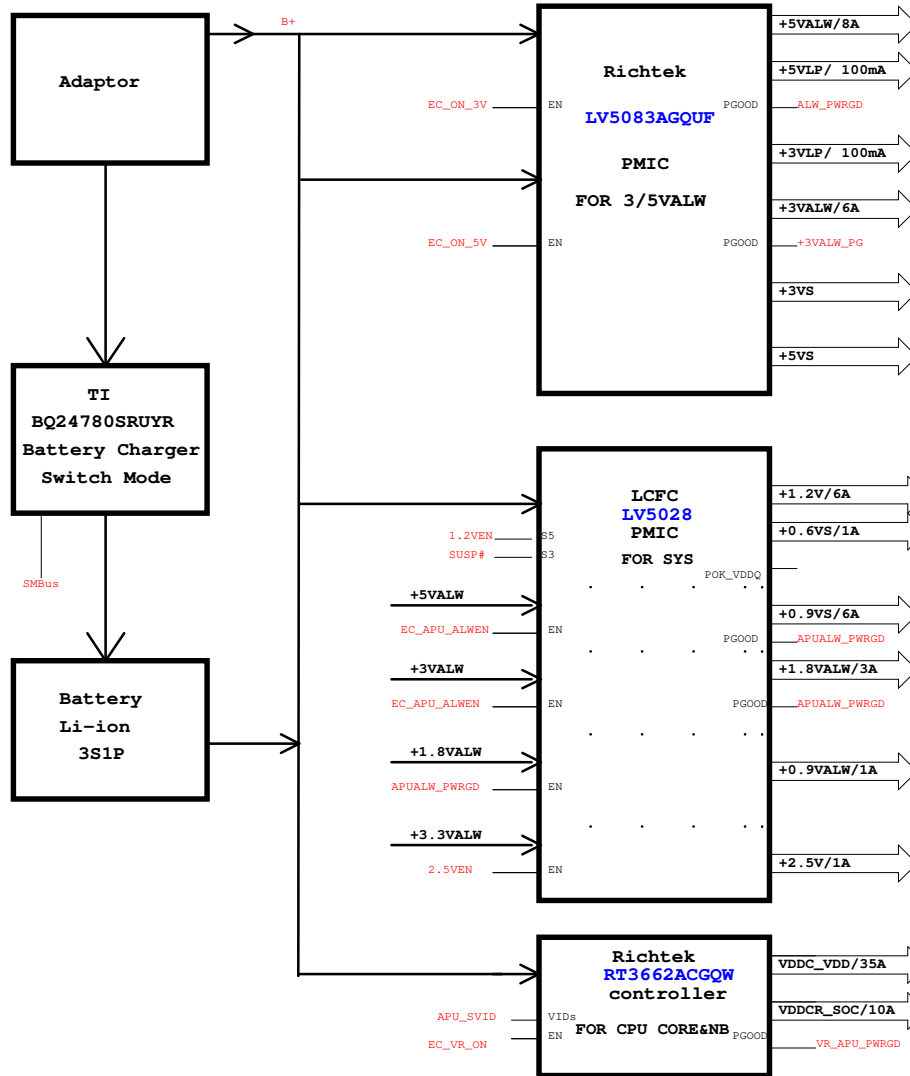


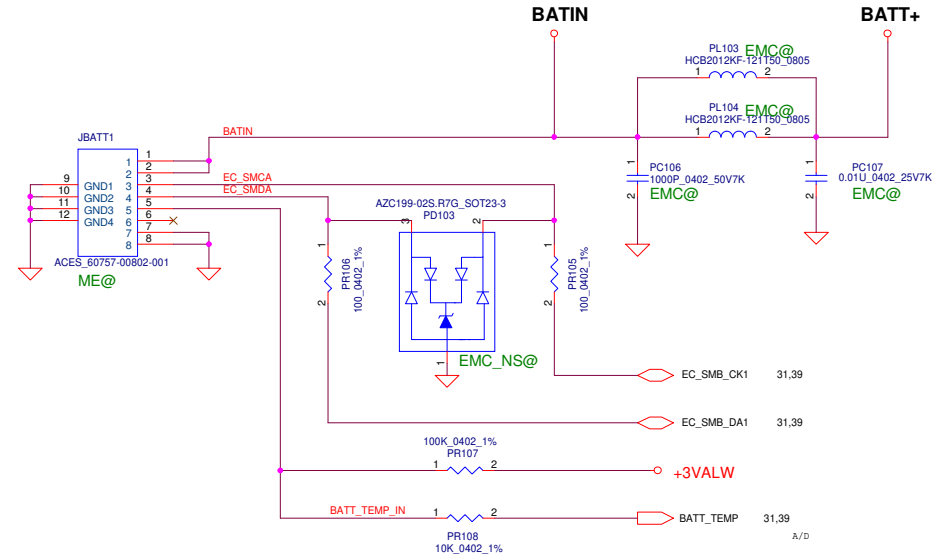
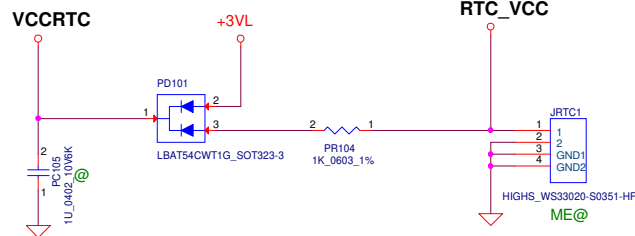
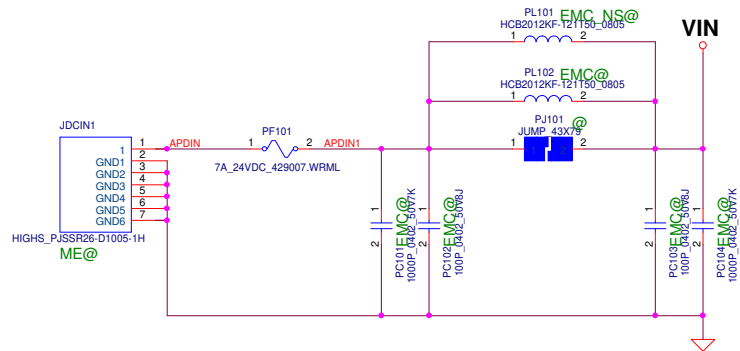
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				Date: Thursday, December 27, 2018	Sheet 36 of 44

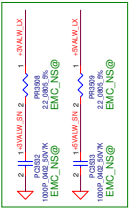
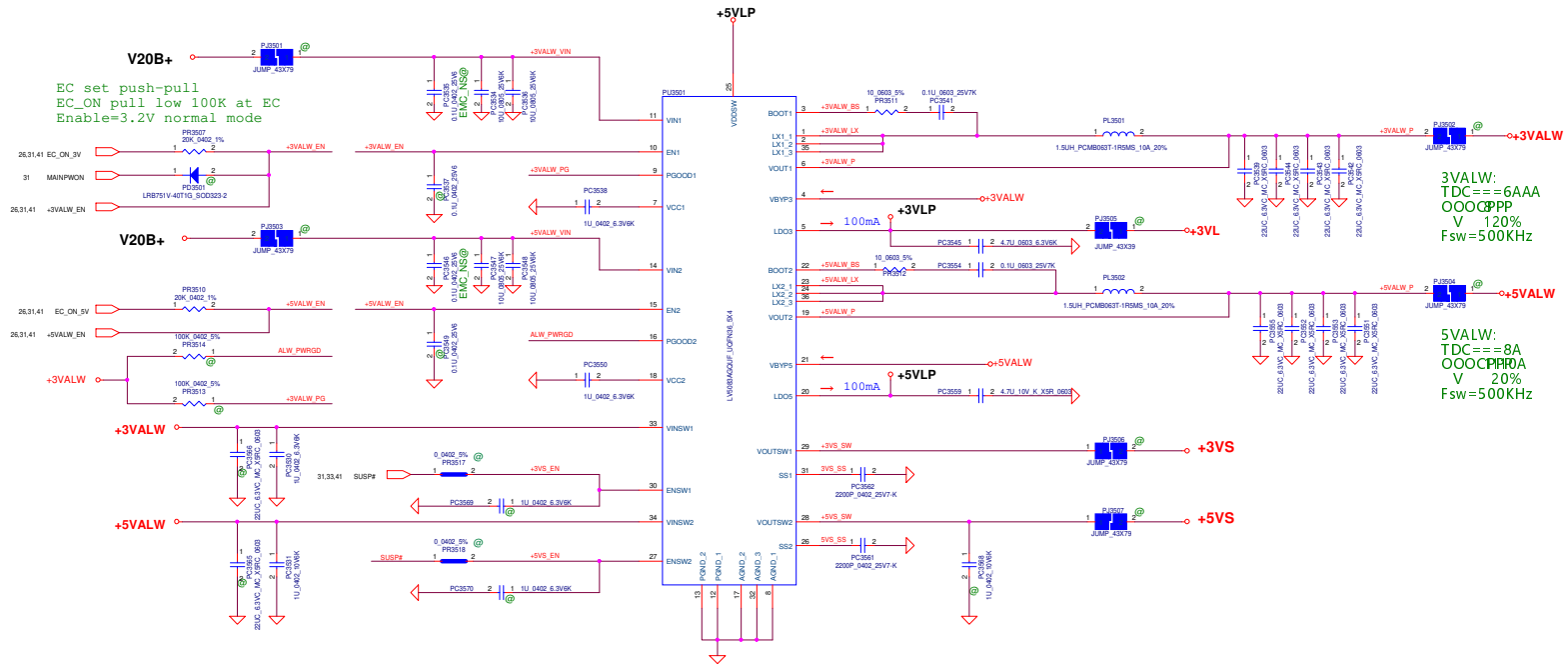


Rev 0.3

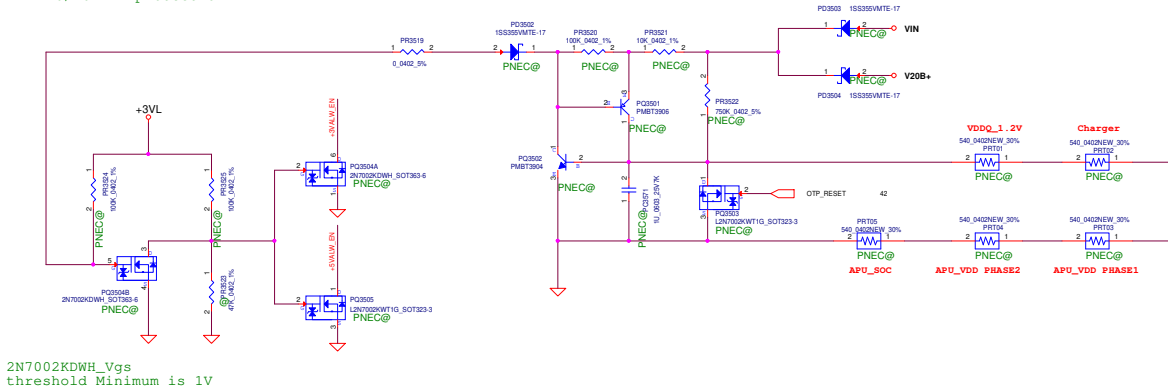


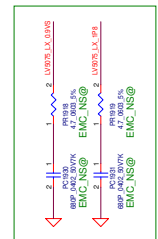
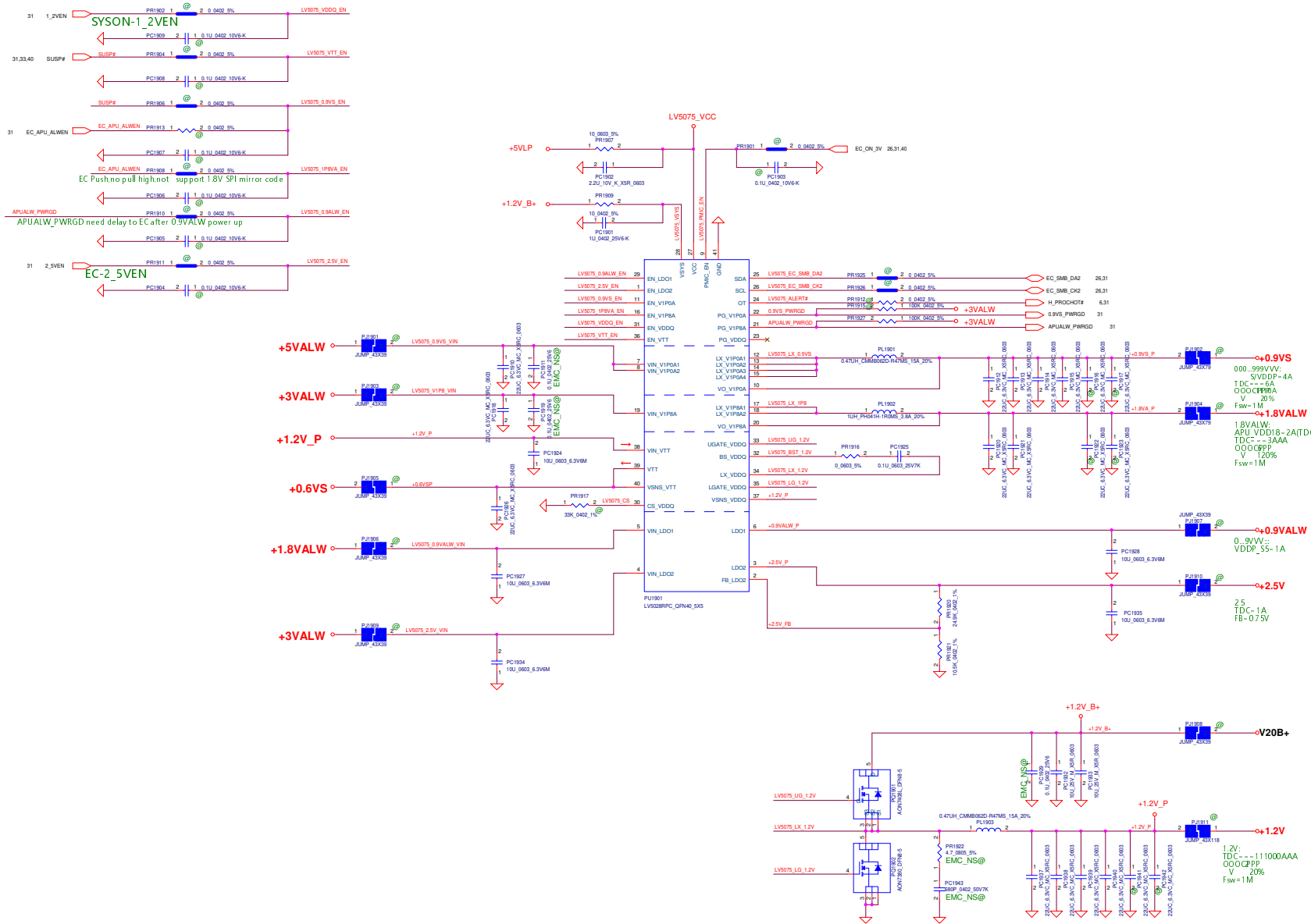


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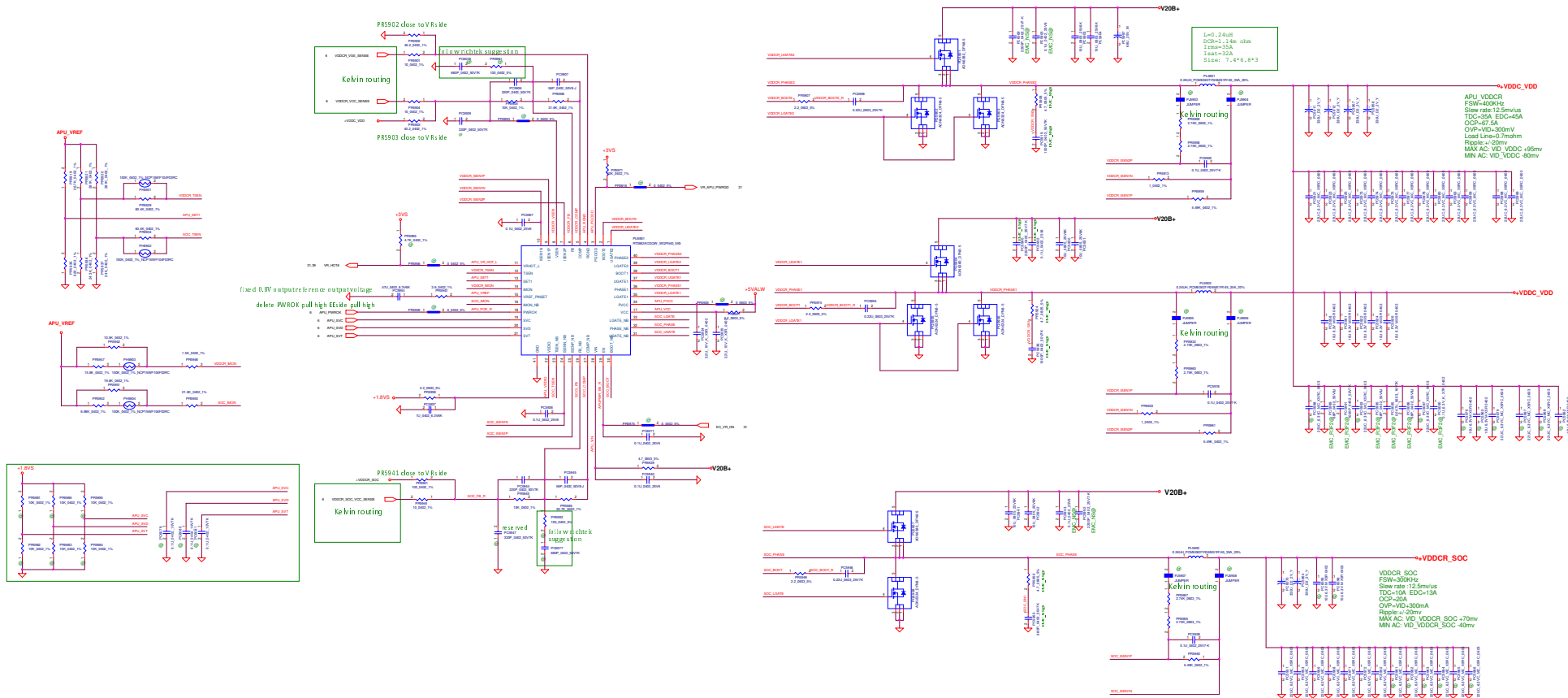
PTC
DC/DC FET protection





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PWR-VDDCR/SOC		Revision	1.370 APC